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2	15	(716/21.ccls. and ((offset or shift or move or shrink) same (line or segment))) and ((delet\$4 or remov\$4 or eliminat\$4) with (vertex or verticies or interconnect\$5 or locus or cluster or point))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/11/01 11:38
-	24	yoshizawa-keiji.in.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/31 18:08
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-	126	(opc or (optical with (process or proximity) with correction)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4 ))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 21:27
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-	45	((optical with (process or proximity) with correction) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4 )))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 20:40

-	44	((optical with (process or proximity) with correction)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4 ))) and (line or segment)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 19:59
-	565	716/21.ccls.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 20:40
-	162	716/21.ccls. and ((offset or shift or move or shrink) same (line or segment))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 21:26
-	54	(716/21.ccls. and ((offset or shift or move or shrink) same (line or segment))) and ((delet\$4 or remov\$4 or eliminat\$4) same (vertex or verticies or interconnect\$5 or locus or cluster or point))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 20:43
-	15	(716/21.ccls. and ((offset or shift or move or shrink) same (line or segment))) and ((delet\$4 or remov\$4 or eliminat\$4) with (vertex or verticies or interconnect\$5 or locus or cluster or point))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/11/01 11:37
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-	511	(optical with (process or proximity) with correction) and (proximity with effect with correction)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/10/29 21:26
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-	14	((optical with (process or proximity) with correction) and (proximity with effect with correction)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4 ))) and (line or segment)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/11/01 11:37
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-	30	((optical with (process or proximity) with recognition)) and ((node or locus or vertex or verticies or intersection) same (detect\$5 or find\$3 or locate\$4)) and ((node or locus or vertex or verticies or intersection) same (delet\$5 or eras\$3 or remov\$4 ))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/11/01 10:32
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# Results of Search "L2"

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1	US 20040209176 A1	20041021	Model-based data conversion	430/5	430/322; 716/19; 716/21
2	US 20040161679 A1	20040819	Full sized scattering bar alt-PSM technique for IC manufacturing in sub-resolution era	430/5	716/19; 716/21
3	US 20020160278 A1	20021031	Method for designing photolithographic reticle layout, reticle, and photolithographic process	430/5	430/322; 716/19; 716/21
4	US 20020132174 A1	20020919	Self-aligned fabrication technique for tri-tone attenuated phase-shifting masks	430/5	430/311; 430/312; 430/313; 430/394; 716/21
5	US 20020015899 A1	20020207	Hybrid phase-shift mask	430/5	430/322; 716/19; 716/21
6	US 6792590 B1	20040914	Dissection of edges with projection points in a fabrication layout for correcting proximity effects	716/19	430/5; 716/21
7	US 6785879 B2	20040831	Model-based data conversion	716/21	430/5; 716/19; 716/7; 716/8
8	US 6711732 B1	20040323	Full sized scattering bar alt-PSM technique for IC manufacturing in sub-resolution era	716/19	716/21

	Document ID	Issue Date	Title	Current OR	Current XRef
9	US 6625801 B1	20030923	Dissection of printed edges from a fabrication layout for correcting proximity effects	716/19	716/21
10	US 6546543 B1	20030408	Method of displaying, inspecting and modifying pattern for exposure	716/21	
11	US 6543045 B2	20030401	Method for detecting and automatically eliminating phase conflicts on alternating phase masks	716/21	716/19; 716/20
12	US 6539521 B1	20030325	Dissection of corners in a fabrication layout for correcting proximity effects	716/4	716/19; 716/21
13	US 6493866 B1	20021210	Phase-shift lithography mapping and apparatus	716/21	430/396; 430/5; 716/19; 716/4
14	US 5124927 A	19920623	Latent-image control of lithography tools	700/121	250/491.1; 356/394; 356/401; 702/94; 716/21
15	US 4559603 A	19851217	Apparatus for inspecting a circuit pattern drawn on a photomask used in manufacturing large scale integrated circuits	716/5	250/491.1; 250/492.2; 257/E21.21 1; 356/237.5; 356/394; 716/21

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 20040191650 A1	20040930	Phase shift masking for complex patterns with proximity adjustments	430/5	716/19
2	US 20030126582 A1	20030703	Pattern correction method and manufacturing method of semiconductor device	716/21	700/121; 716/19
3	US 20030023939 A1	20030130	METHOD AND APPARATUS FOR ANALYZING A LAYOUT USING AN INSTANCE-BASED REPRESENTATION	716/3	716/19; 716/4; 716/5; 716/8
4	US 20020127479 A1	20020912	Phase shift masking for complex patterns with proximity adjustments	430/5	
5	US 20020026624 A1	20020228	Correction of layout pattern data during semiconductor patterning process	716/11	716/10; 716/4
6	US 6792590 B1	20040914	Dissection of edges with projection points in a fabrication layout for correcting proximity effects	716/19	430/5; 716/21
7	US 6777138 B2	20040817	Mask product made by selection of evaluation point locations based on proximity effects model amplitudes for correcting proximity effects in a fabricat layout	430/5	

	Document ID	Issue Date	Title	Current OR	Current XRef
8	US 6733929 B2	20040511	Phase shift masking for complex patterns with proximity adjustments	430/5	430/30; 716/19
9	US 6687885 B2	20040203	Correction of layout pattern data during semiconductor patterning process	716/5	716/11; 716/19
10	US 6625801 B1	20030923	Dissection of printed edges from a fabrication layout for correcting proximity effects	716/19	716/21
11	US 6560766 B2	20030506	Method and apparatus for analyzing a layout using an instance-based representation	716/19	716/11; 716/17; 716/21; 716/4; 716/5; 716/8
12	US 6539521 B1	20030325	Dissection of corners in a fabrication layout for correcting proximity effects	716/4	716/19; 716/21
13	US 6453457 B1	20020917	Selection of evaluation point locations based on proximity effects model amplitudes for correcting proximity effects in a fabrication layout	716/19	430/5; 716/20
14	US 5923566 A	19990713	Phase shifted design verification routine	716/21	430/311; 430/322; 430/5

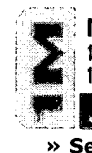


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**1 An automated system for LSI fine pattern inspection based on comparison of SEM images and CAD data**
*Ito, M.;*

 Robotics and Automation, 1995. Proceedings., 1995 IEEE International Conference on , Volume: 1 , 21-27 May 1995  
 Pages:544 - 549 vol.1

[\[Abstract\]](#)    [\[PDF Full-Text \(504 KB\)\]](#)    **IEEE CNF**
**2 HARP: FORTRAN to silicon [compilation system]**
*Tanaka, T.; Kobayashi, T.; Karatsu, O.;*

 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 8 , Issue: 6 , June 1989  
 Pages:649 - 660

[\[Abstract\]](#)    [\[PDF Full-Text \(992 KB\)\]](#)    **IEEE JNL**
**3 The Outline Procedure in Pattern Data Preparation for Vector-Scan Electron-Beam Lithography**
*Komatsu, K.; Suzuki, M.;*

 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 6 , Issue: 1 , January 1987  
 Pages:145 - 151

[\[Abstract\]](#)    [\[PDF Full-Text \(888 KB\)\]](#)    **IEEE JNL**
**4 An ichnographic two-dimensional analysis of the MOS LSI mask layout pattern**
*Natori, K.;*

Solid-State Circuits, IEEE Journal of , Volume: 21 , Issue: 3 , Jun 1986

Pages:457 - 463

[\[Abstract\]](#) [\[PDF Full-Text \(640 KB\)\]](#) IEEE JNL

---

**5 New approach to resolution limit and advanced image formation techniques in optical lithography**

*Fukuda, H.; Imai, A.; Terasawa, T.; Okazaki, S.;*

Electron Devices, IEEE Transactions on , Volume: 38 , Issue: 1 , Jan. 1991

Pages:67 - 75

[\[Abstract\]](#) [\[PDF Full-Text \(864 KB\)\]](#) IEEE JNL

---

**6 An effective fault simulation method for core based LSI**

*Yoshida, T.; Shimoda, R.; Mizokawa, T.; Hirayama, K.;*

Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian , 17-19 Nov. 1997

Pages:116 - 121

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) IEEE CNF

---

**7 Studies on defect inspectivity and printability by using programmed defect X-ray mask**

*Watanabe, H.; Kikuchi, Y.; Marumoto, K.; Matsui, Y.; Yabe, H.; Aya, S.; Okada, Takeuchi, N.;*

Microprocesses and Nanotechnology Conference, 1999. Digest of Papers.

Microprocesses and Nanotechnology '99. 1999 International , 6-8 July 1999

Pages:12 - 13

[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) IEEE CNF

---

**8 Subhalf-micron gate GaAs MESFET process using phase-shifting-mask technology**

*Kimura, T.; Saito, T.; Jinbo, H.; Ichioka, T.; Inokuchi, K.; Yamashita, Y.; Sano,*

Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1991. Technical Digest, 1991., 13th Annual , 20-23 Oct. 1991

Pages:281 - 284

[\[Abstract\]](#) [\[PDF Full-Text \(200 KB\)\]](#) IEEE CNF

---

**9 Feature Size Limit of Liftoff Metallization Technology**

*Homma, Y.; Yajima, A.; Harada, S.;*

Solid-State Circuits, IEEE Journal of , Volume: 17 , Issue: 2 , Apr 1982

Pages:142 - 147

[\[Abstract\]](#) [\[PDF Full-Text \(1096 KB\)\]](#) IEEE JNL

---

**10 A means of reducing custom LSI interconnection requirements**

*Calhoun, D.F.; McNamee, L.P.;*

Solid-State Circuits, IEEE Journal of , Volume: 7 , Issue: 5 , Oct 1972

Pages:395 - 404

[\[Abstract\]](#) [\[PDF Full-Text \(1208 KB\)\]](#) IEEE JNL

---

**11 Fabrication and characteristics of NbN-based Josephson junctions**

**logic LSI circuits**

*Yano, S.; Tarutani, Y.; Mori, H.; Yamada, H.; Hirano, M.; Kawabe, U.;*  
Magnetics, IEEE Transactions on , Volume: 23 , Issue: 2 , Mar 1987  
Pages:1472 - 1475

[\[Abstract\]](#) [\[PDF Full-Text \(688 KB\)\]](#) **IEEE JNL**

---

**12 Inspection of critical dimension- and transmission uniformity of coil patterns by DUV imaging and regression algorithm**

*Yamashita, K.; Yamaguchi, S.;*  
Microprocesses and Nanotechnology Conference, 2000 International , 11-13 J  
2000  
Pages:256 - 257

[\[Abstract\]](#) [\[PDF Full-Text \(88 KB\)\]](#) **IEEE CNF**

---

**13 EYESEE: A machine vision system for inspection of integrated circuit chips**

*Baird, M.;*  
Robotics and Automation. Proceedings. 1985 IEEE International Conference  
on , Volume: 2 , Mar 1985  
Pages:444 - 448

[\[Abstract\]](#) [\[PDF Full-Text \(680 KB\)\]](#) **IEEE CNF**

---

**14 A new inspection method for PSM on DUV inspection light source**

*Isomura, I.; Tsuchiya, H.; Sugihara, S.; Yamashita, K.; Tabata, M.;*  
Microprocesses and Nanotechnology Conference, 2001 International , 31 Oct.-  
Nov. 2001  
Pages:64 - 65

[\[Abstract\]](#) [\[PDF Full-Text \(136 KB\)\]](#) **IEEE CNF**

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**1 High accurate optical proximity correction under the influences of le aberration in 0.15  $\mu$ m logic process**

Harazaki, K.; Hasegawa, Y.; Shichijo, Y.; Tabuchi, H.; Fujii, K.;

Microprocesses and Nanotechnology Conference, 2000 International , 11-13 J 2000

Pages:14 - 15

[\[Abstract\]](#)   [\[PDF Full-Text \(96 KB\)\]](#)   IEEE CNF
**2 Precise patterning technique for Nb junctions using optical proximity correction**

Aoyagi, M.; Nakagawa, H.; Sato, H.; Akoh, H.;

Applied Superconductivity, IEEE Transactions on , Volume: 11 , Issue: 1 , Mar 2001

Pages:381 - 384

[\[Abstract\]](#)   [\[PDF Full-Text \(376 KB\)\]](#)   IEEE JNL
**3 Hierarchical optical proximity correction on contact hole layers**

Yamamoto, K.; Kobayashi, S.; Uno, T.; Kotani, T.; Tanaka, S.; Inoue, S.;

Watanabe, S.; Higurashi, H.;

Microprocesses and Nanotechnology Conference, 2000 International , 11-13 J 2000

Pages:40 - 41

[\[Abstract\]](#)   [\[PDF Full-Text \(100 KB\)\]](#)   IEEE CNF
**4 A 5- $\mu$ m<sup>2</sup> full-CMOS cell for high-speed SRAMs utilizing a optical-proximity-effect correction (OPC) technology**

Ueshima, M.; Mano, M.; Yoneda, Y.; Ichikawa, T.; Tsudaka, K.; Takahashi, H.

*Yamamura, I.; Yabuta, M.; Motoyoshi, M.;*  
VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-  
June 1996  
Pages:146 - 147

[\[Abstract\]](#)   [\[PDF Full-Text \(240 KB\)\]](#)   IEEE CNF

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**5 A cost-driven lithographic correction methodology based on off-the-sizing tools**

*Gupta, P.; Kahng, A.B.; Sylvester, D.; Yang, J.;*  
Design Automation Conference, 2003. Proceedings , 2-6 June 2003  
Pages:16 - 21

[\[Abstract\]](#)   [\[PDF Full-Text \(701 KB\)\]](#)   IEEE CNF

---

**6 Investigation of optical proximity correction (OPC) and non-uniform on the performance of resistivity and linewidth measurements**

*Smith, S.; Walton, A.J.; Fallon, M.;*  
Microelectronic Test Structures, 1999. ICMTS 1999. Proceedings of the 1999  
International Conference on , 15-18 March 1999  
Pages:161 - 166

[\[Abstract\]](#)   [\[PDF Full-Text \(392 KB\)\]](#)   IEEE CNF

---

**7 Automatic proximity correction for 0.35  $\mu\text{m}$  I-line photolithography**

*Garofalo, J.; Low, K.K.; Otto, O.; Pierrat, C.; Vasudev, P.K.; Yuan, C.;*  
Numerical Modeling of Processes and Devices for Integrated Circuits, 1994. NI  
V., International Workshop on , 5-6 June 1994  
Pages:92 - 94

[\[Abstract\]](#)   [\[PDF Full-Text \(176 KB\)\]](#)   IEEE CNF

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**8 Practical applications of 2-D optical proximity corrections for enhanced performance of 0.25  $\mu\text{m}$  random logic devices**

*Chuang, H.; Gilbert, P.; Grobman, W.; Kling, M.; Lucas, K.; Reich, K.; Roman,  
Travis, E.; Tsui, P.; Vuong, T.; West, J.;*  
Electron Devices Meeting, 1997. Technical Digest., International , 7-10 Dec. 1  
Pages:483 - 486

[\[Abstract\]](#)   [\[PDF Full-Text \(784 KB\)\]](#)   IEEE CNF

---

**9 Identify Optical Proximity Correction (OPC) issue in 0.13  $\mu\text{m}$  technology development**

*Zhi Hong Mai; Benjamin Lau; Gang Qian; Jian Jun Shi; Ran He; Jessica Chin;*  
Physical and Failure Analysis of Integrated Circuits, 2003. IPFA 2003. Proceed  
of the 10th International Symposium on the , 7-11 July 2003  
Pages:s199 - s201

[\[Abstract\]](#)   [\[PDF Full-Text \(425 KB\)\]](#)   IEEE CNF

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**10 A little light magic [optical lithography]**

*Schellenberg, F.;*  
Spectrum, IEEE , Volume: 40 , Issue: 9 , Sep 2003

Pages:34 - 39

[\[Abstract\]](#) [\[PDF Full-Text \(1216 KB\)\]](#) [\[Full-Text HTML\]](#) **IEEE JNL**

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**11 An object-based approach to optical proximity correction**

*Changqi Yang; Xianlong Hong; Weimin Wu; Yici Cai; Rui Shi;*

ASIC, 2001. Proceedings. 4th International Conference on , 23-25 Oct. 2001  
Pages:206 - 209

[\[Abstract\]](#) [\[PDF Full-Text \(315 KB\)\]](#) **IEEE CNF**

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**12 The selection and creation of the rules in rules-based optical proximity correction**

*Rui Shi; Yici Cai; Xianlong Hong; Weimin Wu; Changqi Yang;*

ASIC, 2001. Proceedings. 4th International Conference on , 23-25 Oct. 2001  
Pages:50 - 53

[\[Abstract\]](#) [\[PDF Full-Text \(390 KB\)\]](#) **IEEE CNF**

---

**13 Low energy e-beam proximity lithography (LEEPL)**

*Utsumi, T.;*

Microprocesses and Nanotechnology Conference, 1999. Digest of Papers.

Microprocesses and Nanotechnology '99. 1999 International , 6-8 July 1999

Pages:32 - 33

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) **IEEE CNF**

---

**14 Photomasks for advanced lithography**

*Smith, W.; Tybula, W.;*

Electronics Manufacturing Technology Symposium, 1997., Twenty-First IEEE/C International , 13-15 Oct. 1997

Pages:342 - 345

[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) **IEEE CNF**

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**15 Layout design methodologies for sub-wavelength manufacturing**

*Rieger, M.L.; Mayhew, J.P.; Panchapakesan, S.;*

Design Automation Conference, 2001. Proceedings , 18-22 June 2001

Pages:85 - 88

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) **IEEE CNF**

---

**16 A statistical gate CD control including OPC**

*Misaka, A.; Goda, A.; Odanaka, S.; Kobayashi, S.; Watanabe, H.;*

VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on , 9-1 June 1998

Pages:170 - 171

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) **IEEE CNF**

---

**17 Application of full chip OPC to quarter micron logic device**

*Kyune-Jin Shim; Ki-Yeop Park; Won Gyu Lee; Dai-Hoon Lee;*

VLSI and CAD, 1999. ICVC '99. 6th International Conference on , 26-27 Oct. .

Pages:171 - 173

[\[Abstract\]](#) [\[PDF Full-Text \(144 KB\)\]](#) IEEE CNF

---

**18 Advanced gate etching for accurate CD control for 130-nm node AS manufacturing**

*Nagase, M.; Tokashiki, K.;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 17 , Issue: 3 , 2004

Pages:281 - 285

[\[Abstract\]](#) [\[PDF Full-Text \(608 KB\)\]](#) IEEE JNL

---

**19 Level-specific lithography optimization for 1-Gb DRAM**

*Wong, A.K.; Ferguson, R.; Mansfield, S.; Molless, A.; Samuels, D.; Schuster, Thomas, A.;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 13 , Issue: 1 , 2000

Pages:76 - 87

[\[Abstract\]](#) [\[PDF Full-Text \(512 KB\)\]](#) IEEE JNL

---

**20 248nm lithography of 2D photonic crystal waveguide with optical proximity correction**

*Teo, H.G.; Yu, M.B.; Doan, M.T.; Singh, J.; Sun, H.Q.; Liu, A.Q.;*

Biophotonics/Optical Interconnects and VLSI Photonics/WBM Microcavities, 20 Digest of the LEOS Summer Topical Meetings , 28-30 June 2004

Pages:87 - 88

[\[Abstract\]](#) [\[PDF Full-Text \(374 KB\)\]](#) IEEE CNF

---

**21 Optical proximity correction (OPC)-friendly maze routing**

*Li-Da Huang; Wong, M.D.F.;*

Design Automation Conference, 2004. Proceedings. 41st , June 7-11, 2004

Pages:186 - 191

[\[Abstract\]](#) [\[PDF Full-Text \(475 KB\)\]](#) IEEE CNF

---

**22 Test structure for fixing OPC of 200 nm pitch via chain using inner : outer dummy via array**

*Nasuno, T.; Matsubara, Y.; Minami, A.; Uchida, N.; Kobayashi, H.; Aoyama, H. Tsuda, H.; Tsujita, K.; Wakamiya, W.; Kobayashi, N.;*

Microelectronic Test Structures, 2004. Proceedings. ICMTS '04. The International Conference on , 22-25 March 2004

Pages:23 - 28

[\[Abstract\]](#) [\[PDF Full-Text \(563 KB\)\]](#) IEEE CNF

---

**23 A 0.11  $\mu$ m CMOS technology with copper and very-low-k interconnects for high-performance system-on-a-chip cores**

*Takao, Y.; Kudo, H.; Mitani, J.; Kotani, Y.; Yamaguchi, S.; Yoshie, K.; Kawano, Nagano, T.; Yamamura, I.; Uematsu, M.; Nagashima, N.; Kadomura, S.;*

Electron Devices Meeting, 2000. IEDM Technical Digest. International , 10-13

2000  
Pages:559 - 562

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) IEEE CNF

---

**24 A high performance 0.13  $\mu\text{m}$  SOI CMOS technology with Cu interconnects and low-k BEOL dielectric**

*Smeys, P.; McGahay, V.; Yang, I.; Adkisson, J.; Beyer, K.; Bula, O.; Chen, Z.; Chu, B.; Culp, J.; Das, S.; Eckert, A.; Hadel, L.; Hargrove, M.; Herman, J.; Lii Mann, R.; Maciejewski, E.; Narasimha, S.; O'Neil, P.; Rauch, S.; Ryan, D.; Toomey, J.; Tsou, L.; Varekamp, P.; Wachnik, R.; Wagner, T.; Wu, S.; Yu, C.; Agnello, P.; Connolly, J.; Crowder, S.; Davis, C.; Ferguson, R.; Sekiguchi, A.; L.; Goldblatt, R.; Chen, T.C.;*

VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on , 13-June 2000

Pages:184 - 185

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) IEEE CNF

---

**25 An efficient rule-based OPC approach using a DRC tool for 0.18  $\mu\text{m}$**

*Ji-Soong Park; Chul-Hong Park; Sang-Uhk Rhie; Yoo-Hyon Kim; Moon-Hyun Y Jeong-Taek Kong; Hyung-Woo Kim; Sun-Il Yoo;*

Quality Electronic Design, 2000. ISQED 2000. Proceedings. IEEE 2000 First International Symposium on , 20-22 March 2000

Pages:81 - 85

[\[Abstract\]](#) [\[PDF Full-Text \(564 KB\)\]](#) IEEE CNF

---

**26 Efficient full-chip yield analysis methodology for OPC-corrected VLS designs**

*Axelrad, V.; Cobb, N.; O'Brien, M.; Boksha, V.; Do, T.; Donnelly, T.; Granik, Y Sahouria, E.; Balasinski, A.;*

Quality Electronic Design, 2000. ISQED 2000. Proceedings. IEEE 2000 First International Symposium on , 20-22 March 2000

Pages:461 - 466

[\[Abstract\]](#) [\[PDF Full-Text \(212 KB\)\]](#) IEEE CNF

---

**27 Subwavelength lithography (PSM, OPC)**

*Terasawa, T.;*

Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia South Pacific , 25-28 Jan. 2000

Pages:295 - 300

[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) IEEE CNF

---

**28 A manufacturable 0.30  $\mu\text{m}$  gate CMOS technology for high speed microprocessors**

*Appel, A.; Crank, S.; Kim, Y.; Scharrer, C.; Spratt, D.; Strong, B.; Yao, M.; Tigelaar, H.; Melanson, R.;*

VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-June 1996

Pages:220 - 221



[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) IEEE CNF

---

**29 Advanced physical models for mask data verification and impacts on physical layout synthesis**

*Qi-De Qian; Tan, S.X.-D.;*

Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on , 24-26 March 2003

Pages:125 - 130

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) IEEE CNF

---

**30 Process proximity correction by using neural networks**

*Kyoung-Ah Jeon; Ji-Yong Yoo; Jun-Taek Park; Hyeongsoo-Kim; Ilsin An; Hye-Oh;*

Microprocesses and Nanotechnology Conference, 2002. Digest of Papers.

Microprocesses and Nanotechnology 2002. 2002 International , 6-8 Nov. 2002

Pages:256 - 257

[\[Abstract\]](#) [\[PDF Full-Text \(191 KB\)\]](#) IEEE CNF

---

**31 Study on the optimization of high transmittance attenuated phase-shifting mask by design of experiment**

*Wen-an Leong; Hsien-yun Lin; Wen-long Yeh;*

Microprocesses and Nanotechnology Conference, 2002. Digest of Papers.

Microprocesses and Nanotechnology 2002. 2002 International , 6-8 Nov. 2002

Pages:106

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) IEEE CNF

---

**32 Highly manufacturable 32 Mb ULP-SRAM technology by using dual process for 1.5 V Vcc operation**

*Kim, D.H.; Kim, S.J.; Hwang, B.J.; Seo, S.H.; Choi, J.H.; Lee, H.S.; Yang, W.; Kim, M.S.; Kwak, K.H.; Lee, J.Y.; Joo, J.Y.; Kim, J.H.; Koh, K.; Park, S.H.; Ho J.I.;*

VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on , 11-June 2002

Pages:118 - 119

[\[Abstract\]](#) [\[PDF Full-Text \(378 KB\)\]](#) IEEE CNF

---

**33 A 100 nm CMOS technology with "sidewall-notched" 40 nm transistor and SiC-capped Cu/VLK interconnects for high performance microprocessor applications**

*Nakai, S.; Takao, Y.; Otsuka, S.; Sugiyama, K.; Ohta, H.; Yamanoue, A.; Iriya, Y.; Nanjyo, R.; Sekino, S.; Nagai, H.; Naitoh, K.; Nakamura, R.; Sambonsugi, Tagawa, Y.; Horiguchi, N.; Yamamoto, T.; Kojima, M.; Satoh, S.; Sugatani, S. Sugii, T.; Kase, M.; Suzuki, K.; Nakaishi, M.; Miyajima, M.; Ohba, T.; Hanyu, Yanai, K.;*

VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on , 11-June 2002

Pages:66 - 67

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) [IEEE CNF](#)

---

**34 Sub-1 /spl mu/m/sup 2/ high density embedded SRAM technology 100 nm generation SOC and beyond**

*Tomita, K.; Hashimoto, K.; Inbe, T.; Oashi, T.; Tsukamoto, K.; Nishioka, Y.; Matsuura, M.; Eimori, T.; Inuishi, M.; Miyanaga, I.; Nakamura, M.; Kishimoto, Yamada, T.; Eriguchi, K.; Yuasa, H.; Satake, T.; Kajiya, A.; Ogura, M.;*  
VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on , 11-June 2002  
Pages:14 - 15

[\[Abstract\]](#) [\[PDF Full-Text \(373 KB\)\]](#) [IEEE CNF](#)

---

**35 Layout manufacturability analysis using rigorous 3-d topography simulation**

*Strojwas, A.J.; Zhengrong Zhu; Ciplickas, D.; Xiaolei Li;*  
Semiconductor Manufacturing Symposium, 2001 IEEE International , 8-10 Oct 2001  
Pages:263 - 266

[\[Abstract\]](#) [\[PDF Full-Text \(489 KB\)\]](#) [IEEE CNF](#)

---

**36 Level-specific strategy of KrF microlithography for 130 nm DRAMs**

*Inoue, S.; Asano, M.; Hosaka, K.; Sutani, T.; Azuma, T.; Kawamura, D.; Kobayashi, M.; Miyoshi, S.; Kanemitsu, H.; Tanaka, S.; Kotani, T.; Tabata, Y., Tsuchida, K.; Kohyama, Y.; Kawamura, E.;*  
Electron Devices Meeting, 1999. IEDM Technical Digest. International , 5-8 Dec 1999  
Pages:809 - 812

[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) [IEEE CNF](#)

---

**37 Applications of control and signal processing to the microlithography process**

*Schaper, C.D.; Kailath, T.; El-Awady, K.; Tay, A.;*  
Industrial Electronics Society, 1999. IECON '99 Proceedings. The 25th Annual Conference of the IEEE , Volume: 1 , 29 Nov.-3 Dec. 1999  
Pages:1 - 5 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) [IEEE CNF](#)

---

**38 Accurate resist profile simulation for large area OPC**

*Inui, H.; Ohta, T.;*  
Simulation of Semiconductor Processes and Devices, 1999. SISPAD '99. 1999 International Conference on , 6-8 Sept. 1999  
Pages:111 - 114

[\[Abstract\]](#) [\[PDF Full-Text \(224 KB\)\]](#) [IEEE CNF](#)

---

**39 Comparison of mask writing tools and mask simulations for 0.16  $\mu$ m devices**

*Balasinski, A.; Coburn, D.;*  
Advanced Semiconductor Manufacturing Conference and Workshop, 1999

IEEE/SEMI , 8-10 Sept. 1999  
Pages:372 - 377

[\[Abstract\]](#) [\[PDF Full-Text \(428 KB\)\]](#) IEEE CNF

---

**40 Performance of X-ray stepper for next-generation lithography**

*Fukuda, M.; Taguchi, T.;*

Microprocesses and Nanotechnology Conference, 1999. Digest of Papers.

Microprocesses and Nanotechnology '99. 1999 International , 6-8 July 1999

Pages:10 - 11

[\[Abstract\]](#) [\[PDF Full-Text \(188 KB\)\]](#) IEEE CNF

---

**41 Subwavelength lithography and its potential impact on design and**

*Kahng, A.B.; Pati, Y.C.;*

Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999

Pages:799 - 804

[\[Abstract\]](#) [\[PDF Full-Text \(764 KB\)\]](#) IEEE CNF

---

**42 Impact of RSF with variable coefficients for CD variation analysis including OPC**

*Goda, A.; Misaka, A.; Odanaka, S.;*

Statistical Metrology, 1999. IWSM. 1999 4th International Workshop on , 12 J 1999

Pages:62 - 65

[\[Abstract\]](#) [\[PDF Full-Text \(288 KB\)\]](#) IEEE CNF

---

**43 Monte-Carlo Based Optical Proximity Correction For The Half-Tone Phase Shift Mask**

*Yong-Ho Oh; Jai-Cheol Lee; Sungwoo Lim;*

Microprocesses and Nanotechnology Conference, 1998 International , 13-16 J 1998

Pages:62 - 63

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) IEEE CNF

---

**44 Impact of high resolution lithography on IC mask design**

*Pugh, G.; Canning, J.; Roman, B.;*

Custom Integrated Circuits Conference, 1998., Proceedings of the IEEE 1998 , 14 May 1998

Pages:149 - 153

[\[Abstract\]](#) [\[PDF Full-Text \(572 KB\)\]](#) IEEE CNF

---

**45 A 0.15  $\mu$ m KrF lithography for 1 Gb DRAM product using highly prin patterns and thin resist process**

*Ozaki, T.; Azuma, T.; Itoh, M.; Kawamura, D.; Tanaka, S.; Ishibashi, Y.;*

*Shiratake, S.; Kyoh, S.; Kondoh, T.; Inoue, S.; Tsuchida, K.; Kohyama, Y.; O. Y.;*

VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on , 9-1 June 1998

Pages:84 - 85

[\[Abstract\]](#) [\[PDF Full-Text \(444 KB\)\]](#) IEEE CNF

---

**46 Lithography technology development and design rule consideration  
0.4-0.35  $\mu\text{m}$  DRAM semiconductor processes**

*Lee, D.H.-T.; Chang-Ming Dai;*

VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on , 31 May-2 June 1995

Pages:300 - 308

[\[Abstract\]](#) [\[PDF Full-Text \(820 KB\)\]](#) IEEE CNF

---

**47 Optical lithography techniques for 0.25  $\mu\text{m}$  and below: CD control is**

*van den Hove, L.; Ronse, K.; Pforr, R.;*

VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on , 31 May-2 June 1995

Pages:24 - 30

[\[Abstract\]](#) [\[PDF Full-Text \(684 KB\)\]](#) IEEE CNF

---

**48 Electromagnetic fields near a concave perfectly conducting cylindrical  
surface**

*Topuz, E.; Niver, E.; Felsen, L.;*

Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988] , Volume 30 , Issue: 2 , Mar 1982

Pages:280 - 292

[\[Abstract\]](#) [\[PDF Full-Text \(1080 KB\)\]](#) IEEE JNL

---

**49 Electrical CD characterisation of binary and alternating aperture ph  
shifting masks**

*Smith, S.; McCallum, M.; Walton, A.J.; Stevenson, J.T.M.;*

Microelectronic Test Structures, 2002. ICMTS 2002. Proceedings of the 2002 International Conference on , 8-11 April 2002

Pages:7 - 12

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE CNF

---

**50 Exposure tool effects on OPC**

*Detje, M.; Hassmann, J.; Kurth, K.;*

Microprocesses and Nanotechnology Conference, 2002. Digest of Papers.

Microprocesses and Nanotechnology 2002. 2002 International , 6-8 Nov. 2002  
Pages:298

[\[Abstract\]](#) [\[PDF Full-Text \(157 KB\)\]](#) IEEE CNF

---

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**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**51 Practical application of full-feature alternating phase-shifting technology for a phase-aware standard-cell design flow**

Sanie, M.; Cote, M.; Hurat, P.; Malhotra, V.;

Design Automation Conference, 2001. Proceedings, 18-22 June 2001

Pages:93 - 96

[\[Abstract\]](#)   [\[PDF Full-Text \(404 KB\)\]](#)   IEEE CNF
**52 Rigorous modeling of scattered light in EUV cameras**

Krautschik, C.; Ito, M.; Nishiyama, I.;

Microprocesses and Nanotechnology Conference, 2001 International, 31 Oct.-Nov. 2001

Pages:14

[\[Abstract\]](#)   [\[PDF Full-Text \(98 KB\)\]](#)   IEEE CNF
**53 Applications of mathematical systems science to nanolithography of integrated circuits**

Schaper, C.; Kailath, T.;

University/Government/Industry Microelectronics Symposium, 1999. Proceedings of the Thirteenth Biennial, 20-23 June 1999

Pages:120 - 122

[\[Abstract\]](#)   [\[PDF Full-Text \(284 KB\)\]](#)   IEEE CNF
**54 Practical resolution limit of KrF lithography**

Schuster, R.;

VLSI Technology, Systems, and Applications, 1999. International Symposium on, 8-10 June 1999

Pages:123 - 126

[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) IEEE CNF

---

**55 Excellent process control technology for highly manufacturable and performance 0.18  $\mu\text{m}$  CMOS LSIs**

*Nakayama, T.; Asamura, T.; Kako, M.; Murota, M.; Matsumoto, M.; Washizu, Tomose, K.; Kasai, K.; Okayama, Y.; Hashimoto, K.; Ohuchi, K.; Hattori, K.; Shiozawa, J.; Harakawa, H.; Matsuoka, F.; Kinugawa, M.;*

VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on , 9-1 June 1998

Pages:146 - 147

[\[Abstract\]](#) [\[PDF Full-Text \(400 KB\)\]](#) IEEE CNF

---

**56 A manufacturable and modular 0.25  $\mu\text{m}$  CMOS platform technology**

*Tsui, P.; Chuang, H.; Bhat, N.; Travis, E.; Chheda, S.; Grant, J.; Gilbert, P.; C P.; Poon, S.; Kaiser, A.; Anthony, B.; White, T.; West, J.; Vuong, T.; Mattay, Kruth, B.; Perera, A.; Porter, J.; Schippers, M.; Yang, I.; Misra, V.; Venkatesa Nagy, A.; Lii, T.;*

VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on , 9-1 June 1998

Pages:152 - 153

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) IEEE CNF

---

**57 Optical redshifts due to correlations in quasar plasmas**

*Lama, W.; Walsh, P.J.;*

Plasma Science, IEEE Transactions on , Volume: 31 , Issue: 6 , Dec. 2003

Pages:1223 - 1229

[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) IEEE JNL

---

**58 A hybrid technique for combining moment methods with the geometric theory of diffraction**

*Thiele, G.; Newhouse, T.;*

Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988] , Volume 23 , Issue: 1 , Jan 1975

Pages:62 - 69

[\[Abstract\]](#) [\[PDF Full-Text \(664 KB\)\]](#) IEEE JNL

---

**59 Microlithography: trends, challenges, solutions, and their impact on design**

*Wong, A.K.;*

Micro, IEEE , Volume: 23 , Issue: 2 , March-April 2003

Pages:12 - 21

[\[Abstract\]](#) [\[PDF Full-Text \(457 KB\)\]](#) IEEE JNL

---

**60 Comparison of electrical and SEM CD measurements on binary and alternating aperture phase-shifting masks**

*Smith, S.; McCallum, M.; Walton, A.J.; Stevenson, J.T.M.; Lissimore, A.;*

Semiconductor Manufacturing, IEEE Transactions on , Volume: 16 , Issue: 2 ,

2003  
Pages:266 - 272

[\[Abstract\]](#) [\[PDF Full-Text \(829 KB\)\]](#) IEEE JNL

---

**61 A high-resolution contamination-mode inspection method providing complete solution to the inspection challenges for advanced photomask**  
*Bhattacharyya, K.; Yao-Tsu Huang; Kong Son; Den Wang; Liu, L.; Liao, C.H.; Ming Dai; Jyh-Ching Lin;*  
Advanced Semiconductor Manufacturing, 2004. ASMC '04. IEEE Conference and Workshop , 4-6 May 2004  
Pages:285 - 290

[\[Abstract\]](#) [\[PDF Full-Text \(446 KB\)\]](#) IEEE CNF

---

**62 Architecture of a post-OPC silicon verification tool**  
*Xiaolang Yan; Ye Chen; Zheng Shi; Zhijin Chen;*  
ASIC, 2003. Proceedings. 5th International Conference on , Volume: 2 , 21-24 2003  
Pages:1365 - 1368 Vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(383 KB\)\]](#) IEEE CNF

---

**63 A new correction method for dry etch loading effect in photomask fabrication**  
*Won-Tai Ki; Seung-Hune Yang; Seong-Yong Moon; Seong-Woon Choi; Woo-S. Han; Jung-Min Sohn;*  
Microprocesses and Nanotechnology Conference, 2000 International , 11-13 June 2000  
Pages:42 - 43

[\[Abstract\]](#) [\[PDF Full-Text \(140 KB\)\]](#) IEEE CNF

---

**64 A 0.15  $\mu\text{m}$  CMOS foundry technology with 0.1  $\mu\text{m}$  devices for high performance applications**  
*Diaz, C.H.; Chang, M.; Chen, W.; Chiang, M.; Su, H.; Chang, S.; Lu, P.; Hu, C. Pan, K.; Yang, C.; Chen, L.; Su, C.; Wu, C.; Wang, C.H.; Wang, C.C.; Shih, J. Hsieh, H.; Tao, H.; Jang, S.; Yu, M.; Shue, S.; Chen, B.; Chang, T.; Hou, C.; B.K.; Lee, K.H.; Sun, Y.C.;*  
VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on , 13-14 June 2000  
Pages:146 - 147

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) IEEE CNF

---

**65 Feasibility demonstration of 0.18  $\mu\text{m}$  and 0.13  $\mu\text{m}$  optical projection lithography based on CD control calculations**  
*Kee-Ho Kim; Ronse, K.; Yen, A.; Van den Hove, L.;*  
VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-14 June 1996  
Pages:186 - 187

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) IEEE CNF

---

**66 Fabrication of small contact with novel mask design**

*Kang, H.Y.; Lee, J.H.; Cha, D.H.; Moon, S.Y.; Koh, Y.B.;*

VLSI Technology, 1996. Digest of Technical Papers. 1996 Symposium on , 11-June 1996

Pages:184 - 185

[\[Abstract\]](#) [\[PDF Full-Text \(176 KB\)\]](#) IEEE CNF

---

**67 Transistor flaring in deep submicron-design considerations**

*Singhal, V.; Keshav, C.B.; Sumanth, K.G.; Suresh, P.R.;*

Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia South Pacific and the 15th International Conference on VLSI Design. Proceedings , 7-11 Jan. 2002

Pages:299 - 304

[\[Abstract\]](#) [\[PDF Full-Text \(1113 KB\)\]](#) IEEE CNF

---

**68 The double exposure strategy using OPC and simulation and the performance on wafer with sub-0.10  $\mu\text{m}$  design rule in ArF lithography**

*Se-Young Oh; Wan-Ho Kim; Hyoung-Soon Yune; Hee-Bom Kim; Seo-Min Kim, Chang-Nam Ahn; Young-Mog Ham; Ki-Soo Shin;*

Microprocesses and Nanotechnology Conference, 2001 International , 31 Oct.-Nov. 2001

Pages:12 - 13

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) IEEE CNF

---

**69 A novel approach to simulate the effect of optical proximity on MOS parametric yield**

*Balasinski, A.; Gangala, H.; Axelrad, V.; Boksha, V.;*

Electron Devices Meeting, 1999. IEDM Technical Digest. International , 5-8 Dec 1999

Pages:913 - 916

[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) IEEE CNF

---

**70 IC layout and manufacturability: critical links and design flow implications**

*Kahng, A.B.;*

VLSI Design, 1999. Proceedings. Twelfth International Conference On , 7-10 Jan 1999

Pages:100 - 105

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) IEEE CNF

---

**71 Effects of photoresist foreshortening on an advanced Ti/AlCu/Ti metallurgy and W interconnect technology**

*Whiteside, C.; Rutten, M.; Trombley, H.; Landis, H.; Boltz, M.;*

Advanced Semiconductor Manufacturing Conference and Workshop, 1998. 19th IEEE/SEMI , 23-25 Sept. 1998

Pages:332

[\[Abstract\]](#) [\[PDF Full-Text \(440 KB\)\]](#) IEEE CNF



---

**72 Recognition and localization of 3-D natural quadric objects based on active sensing**

*Lee, S.; Hahn, H.;*

Robotics and Automation, 1991. Proceedings., 1991 IEEE International Conference on , 9-11 April 1991

Pages:156 - 161 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(580 KB\)\]](#) [IEEE CNF](#)

---

**73 Object pose estimation based on one-degree-of-freedom sensor**

*Heikkila, T.;*

Intelligent Robots and Systems '90. 'Towards a New Frontier of Applications', Proceedings. IROS '90. IEEE International Workshop on , 3-6 July 1990

Pages:903 - 910 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) [IEEE CNF](#)

---

**74 Neural network proximity effect corrections for electron beam lithography**

*Frye, R.C.; Rietman, E.A.; Cummings, K.D.;*

Systems, Man and Cybernetics, 1990. Conference Proceedings., IEEE International Conference on , 4-7 Nov. 1990

Pages:704 - 706

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) [IEEE CNF](#)

---

**75 Management and control of the electromagnetic compatibility of large range finder target designator systems including thermal imaging sensors, TV sensors and other sensors collocated on stabilized (gimbaled) platforms in proximity to pulsed Nd:YAG lasers**

*Zentner, J.; Thompson, A.; Favors, H.A.; Slobe, D.; Taylor, K.;*

Electromagnetic Compatibility, 1988. Symposium Record. IEEE 1988 International Symposium on , 2-4 Aug. 1988

Pages:465 - 467

[\[Abstract\]](#) [\[PDF Full-Text \(208 KB\)\]](#) [IEEE CNF](#)

---

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